TITLE OF THE INVENTION

Modulator and Demodulator(MODEM)

BACKGROUND OF THE INVENTION

Field of the invention

The present invention relates to a MODEM for data communication via a telephone line between Data Terminal Equipment(DTE) such as a computer and a facsimile apparatus, more particularly to a MODEM selecting an appropriate modulating method from a plurality of modulating methods.

Description of the prior art

Several kinds of modulating methods are available in MODEMs such as frequency modulation, four-phase differential phase shift modulation, quadrature amplitude modulation, and phase amplitude modulation. Selection of these methods depends on a communication speed. Recently, many of MODEMs, for example a MODEM incorporated in a facsimile apparatus switch a modulation/demodulation mode as well as speeds depending on the protocol. It is crucially important to synchronize a timing of mode switch between a transmitter and receiver. In a conventional manner, DTE, a host apparatus of MODEM, selects an operation mode, and the MODEM follows an instruction from the DTE to switch the operation mode.

DTE is connected with MODEM via BUS, and CPU of DTE knows transmitted/received data by reading/writing the transmitting-

data-register and receiving-data-register both are housed by the MODEM. Also the CPU recognizes the present operation of the MODEM by reading the status-displaying-register, and switches an operation mode of the MODEM by writing a mode number into the mode register. The modulating and demodulating portion in the MODEM follows an instruction from the mode register, and reports the status of each operation to the DTE via the status-display-register.

Before ITU (International Telecommunication Union) announced V.34 Standard based on ITU-T Recommendation, all the MODEMs used in the facsimiles were of half-duplex type, and no timing was available for transmitting a waveform simultaneously from both sides of transmitter and receiver. Only either one of the sides thus transmitted a waveform. Therefore, a sequence of signal-transmitting was determined by a protocol such as T.30 Standard.

An operation according to T.30 Standard is explained here:

A previous mode is a receiving mode, and the content of the received data is judged to switch the next mode into transmitting. In this case, DTE judges the received data and instructs the MODEM to switch the mode; however, software process in DTE takes time in anyway and produces a signal gap between the end of receiving signal and start of transmitting signal. When employing a half duplex communication, whatever the signal gap length may be, it will not be a cause of stopping the communication.

On the other hand, when the communication is operated based

on V.34 Standard, the full duplex mode is employed only in communicating through a controlling channel, whereby signals are transmitted simultaneously from both sides. Accordingly, when the previous mode is ended in full-duplex mode of the controlling channel, and suppose the next mode is a receiving mode of a main channel. Then DTE is supposed to judge the data of controlling channel and give an instruction of mode switch to the MODEM.

A problem occurs in the above case: The timing of mode switch depends on an instruction from the DTE side. If processing the transmitted/received data would take time on the DTE side, the MODEM cannot receive the main channel, for the switching from the receiving of control channel of the previous mode to the receiving of main channel of the next mode delays. When a MODEM of a higher speed is employed, processing data volume per hour increases, whereby this kind of problems occur more often.

When the half-duplex MODEM of V.34 Standard is employed, the main channel of one-way communication and the controlling channel of two-way simultaneous communication are switched over alternately. In this case, if a signal gap spans over a specific period (0.1 seconds), an echo-suppressor is recovered, whereby the controlling channel cannot be through the two-way simultaneous communication, and the communication is thus unable to recover. In order to prevent this problem, V.34 Standard specifies the signal gap to be within 70 ms ± 5 ms.

Therefore, a mechanism which shortens the process time is

required in an interface between the MODEM and DTE. However, if the process time can be shortened at the DTE side and switch timing can be spanned less period in proportion to the signal gap length, monitoring the signal gap length requires around ±5 ms accuracy. At the DTE side, a software for monitoring the MODEM status thus requires a top priority, whereby the system design of DTE encounters the difficulty.

SUMMARY OF THE INVENTION

The present invention overcomes the problems proper to conventional methods, and shortens the process time of the interface between the DTE and MODEM as well as switches a mode independently of the DTE's software. The MODEM according to the present invention has these two novelties.

According to the present invention, an object program of the procedure is basically stored in a memory means. Corresponding to the object program execution, an operation mode is switched automatically in accordance with the each procedure specified in advance, and the procedure corresponding to the present operation mode switched from the previous mode is automatically executed. In other words, the MODEM monitors the mode-switch-control for itself and executes the mode switch by itself independently of the the host apparatus, DTE.

The basic structure of the present invention realizes this feature: since the MODEM switches modes by itself, the transfer

efficiency to DTE is increased and a given timing is guaranteed, whereby data communication which requires a delicate timing can be through, a trouble-free communication is secured, and total communication efficiency is increased.

The present invention has various embodiments for this basic structure. First, data storage areas which temporarily store the data transmitted to/from the host apparatus are provided to each operation mode. Accordingly, when the MODEM switches the modes by itself, received data is written into different areas in response to each mode. If a response speed cannot follow the MODEM's communication speed even in a moment, a received data of the next mode is stored in another area of the memory means, the received data of the next mode thus will not overwrite the counterpart of the previous frame.

In another embodiment, a data storage area comprises two areas in pairs corresponding to each operation, one is a command storage area storing commands from the data terminal equipment (DTE), and another is a data storage area storing data from the DTE. When a transmitted data in a data storage area is processed, a command written by the host apparatus into the corresponding command storage area is checked, and an operation follows the command.

Further in another embodiment, the data storage areas of each operation mode has plural banks, and data from the DTE is stored in each bank in the unit of frame. An error-check is

conducted on the stored data from the DTE, and a "data error" is written into a status register, and then the received data which includes errors is canceled. In this embodiment, the data-error is thus not written in the corresponding bank, and a memory capacity is utilized with less waste. Since the result of error-check, i.e. data-error, is still maintained, a notice can be given to the DTE that a data-error is produced.

Still further in another embodiment, a transit time between an end of procedure and a start of next procedure is monitored, and a specified operation mode is to be automatically started when the transit time exceeds a prescribed period. In this embodiment, response-delay to the next mode is thus prevented, where a procedure requires ±5 ms accuracy for monitoring the signal gap length.

In another different embodiment, a received data frame in the MODEM is deframed and analyzed to judge whether the data frame is an RCP (return to control for partial page) frame or not. If the data frame is judged the RCP frame, the operation mode is automatically switched from the main-channel-receiving-mode to the controlling channel mode, whereby preventing to miss a controlling-channel-signal arriving within 75 ms after ending the main channel.

In a separate embodiment, the MODEM analyzes the received data. If the analysis tells that there is an end signal of controlling channel of a special pattern which could not occur in

data transmission, the MODEM switches automatically the operation mode from the controlling channel mode to the main-channel-receiving mode, whereby preventing to miss a main channel signal arriving within 75 ms after ending the controlling channel.

Further in another separate embodiment, the MODEM calculates an error quantity, and specifies the acceptable maximum error quantity. When an error quantity exceeds this acceptable maximum error quantity, a retraining signal is sent to the communication line. The acceptable maximum error quantity may be instructed by the DTE. Therefore, in this embodiment, when quality of received data is even lowered during data transmission, load on the DTE can be reduced and also a quality level can be recovered quickly whereby a total communication can end quickly.

Still in a separate embodiment, a timer is installed, which start counting a prescribed time simultaneously when the MODEM transmits a specified signal to the communication line. When a response signal to the specified signal during the prescribed time is detected, the timer is reset. If the response signal is not detected from the line during the specified time, the DTE is given a notice of abnormal. Therefore, in a normal operation where the response signal is detected from the line, the DTE needs not know about the detection of the response signal, whereby the process is never interfered. The load upon the DTE thus can be reduced comparing with when every monitor result is noticed to the DTE.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram depicting a MODEM according to an embodiment of the present invention.

Fig. 2 depicts a memory structure of a dual port RAM in Fig. 1.

Fig. 3 depicts a memory structure of a channel area required to access a channel block of the present invention.

Fig. 4 details a bit map in the channel command illustrated in Fig. 3.

Fig. 5 details a bit map in the channel status illustrated in Fig. 4.

Fig. 6 depicts a relation between command areas, status areas and banks on the dual port RAM.

Fig. 7 depicts a memory structure detailing a bit map in the command area of the present invention.

Fig. 8 depicts a memory structure detailing a bit map in the status area of the present invention.

Fig. 9 depicts a memory structure showing a transmission interrupt of the present invention.

Fig. 10 depicts a memory structure showing a receiving interrupt of the present invention.

Fig. 11 depicts a situation of error-frame being detected when a received data's frame is checked.

Fig. 12(a) depicts a conventional memory still storing an error-frame after being judged so.

Fig. 12(b) depicts a memory of this invention, which cancels an error-frame when being judged so.

Fig. 13 depicts when an abort is detected in received data.

Fig. 14(a) depicts a conventional memory still storing an error-frame after being judged so.

Fig. 14(b) depicts a memory of this invention, which cancels an error-frame when being judged so.

Fig. 15 is a control flow chart depicting an embodiment of mode switch according to this invention.

Fig. 16 is a receiving side's flow chart depicting a facsimile sequence using a half duplex mode of V.34 Standard according to this invention.

Fig. 17 depicts a mode switch by RCP detection of this invention.

Fig. 18 depicts a sample of timing used in facsimile/data communication in V.34 mode according to this invention.

Fig. 19 depicts a circuit of MODEM used in an embodiment of this invention.

Fig. 20 is an inner block diagram of EQM calculator showed in Fig. 19. (EQM: eye quality monitor)

Fig. 21 is a flow chart to be executed by the controller showed in Fig. 19 in data receiving mode.

Fig. 22 is a sequence diagram outlining a procedure of V.34 half duplex used in this invention.

PREFERRED EMBODIMENTS

Fig. 1 is a block diagram outlining a MODEM used in this embodiment of the present invention. A MODEM 11 modulates and demodulates data. A facsimile controller 12 functions as a host DTE and processes data expansion and data record. The MODEM 11 comprises a line controller 111, an analog FEP 112 (FEP: front end processor), a DSP 113 (DSP:digital signal processor) which digitally processes modulation and demodulation etc., a dual port RAM 114 having two READ/WRITE access ports, and an interrupt controller 115.

The facsimile controller 12 comprises an image reader/recorder 123, an image data compressor/expandor 122, a console 121 including a control panel, a working RAM 124 which temporarily stores image data, and a CPU 125 (central processing unit) which controls operation of the entire apparatus.

A first access port of the dual port RAM 114 is connected to a BUS B1 in the MODEM 11, and a second access port is connected to a BUS B2 in the facsimile controller 12, so that READ/WRITE from the MODEM 11 and facsimile controller 12 can be practiced simultaneously.

The present invention employs the dual port RAM 114 to be disposed between the DTE and MODEM in order to increase data-transmit-efficiency of the interface between the DTE and MODEM as well as reduces time-load on software at the DTE side: The dual port RAM 114 can transmits data in a unit of data-frame which is

an error detecting unit. A buffer area of the frame unit is not limited to one frame but extends to a block area linking plural frames (hereinafter called as a channel block.)

Fig. 2 depicts a memory structure of the dual port RAM 114 shown in Fig. 1. A communication buffer is independently provided to each mode, such as a channel block A to the main channel, a channel block B to the transmitter controlling channel, a channel block C to the receiver controlling channel. Each communication buffer has plural banks 0 – 3. The channel blocks A, B, and C have channel area pointers (CH area pointer) and channel areas (CH area). The CH area pointers have information for accessing the CH area.

Fig. 3 depicts a memory structure required for accessing the channel blocks. A channel command is an area for storing a command which switches a corresponding channel to transmitting mode or receiving mode. A channel status is an area to display the information about an error in transmitting/receiving of the corresponding channel.

Fig. 4 details an example of a bit map in the channel command shown in Fig. 3.

Fig. 5 details an example of a bit map in the channel status shown in Fig. 3.

The MODEM 11 so structured as above is explained here when V.34 half duplex is used in a communication:

An embodiment here shows how to control received data from

the facsimile controller 12 independently in each mode.

When communicating by using V.34 half duplex, a channel of communication comprises a main channel and a controlling channel. The main channel is used for image information in the facsimile communication, and the controlling channel is used for the communication of Phase B control information recommended in T.30 Standard of ITU-T. The main channel uses the channel block A, transmitting of the controlling channel uses the channel block B, and receiving of the controlling channel uses the channel block C.

First, a transmiting-process of controlling channel is described: In Phase B of T.30 Standard, the MODEM 11 sets the channel mode of channel block B at "bit 1" in order to transmit the controlling channel. Data is written into the bank 0 of channel block B. The MODEM 11 recognizes the "bit 1" of Data Full /Empty, confirms the ending of WRITE, reads the data from Bank 0, processes signals including modulation, and transmits data to the communication line. After transmitting data out of Bank 0, the MODEM 11 changes the display bit of Data Full/Empty of Status 0 to "0".

When the display bit of Data Full/Empty of Status 1 which corresponds to Bank 1 is "0", the facsimile controller 12, on the other hand, writes the next data-frame into Bank 1 while the MODEM 11 transmits the data of Bank 0. After completing WRITE, the display bit of Data Full/Empty of Status 1 is changed to "1". The MODEM 11 checks Status 1 after completing the transmission of

Bank 0, and when the display bit of Data Full/Empty is "1" (in other words, the next data-frame was written-in already), the data of Bank 1 is transmitted as same as Bank 0. In the same manner, Bank 2, 3, and 0 in this sequence are transmitted in the unit of data-frame. Although the transmitting command of controlling channel is in execution, when the display bits of Data Full/Empty of Bank status in all Banks are at "0" and no data-frame to be transmitted is available, the MODEM changes transmitting-error-display-bit of channel status B into "1" and gives a notice of an transmitting error of channel block B to the facsimile controller 12.

Second, the receiving process of controlling channel is described: The MODEM 11 sets a channel mode of channel command C at "0" in order to receive the controlling channel, and the MODEM 11 receives as well as demodulates data, confirms that the display bit of Data Full/ Empty of Status 0 which corresponds to Bank 0 of channel block C is "0", and writes one data frame into Bank 0. After completing the write-in, the display bit of Data Full/Empty of Status 0 is changed to "1" (Completing WRITE = READ Ready.) The facsimile controller 12 confirms that the display bit of Data Full/Empty of Status 0 is "1", then reads data out of Bank 0. When the display bit of Data Full/Empty of Bank 1 is "0", the MODEM 11 writes the next data-frame of receiving into Bank 1 while data of Bank 0 is read by the facsimile controller 12. In the same manner, Bank 2, 3 and 0 in this sequence are received and

processed in the unit of data-frame.

Although the receiving command of controlling channel is in execution, when the display bits of Data Full/Empty of Bank status in all Banks are at "1" and no received data-frame can be written into vacant banks of C channel block, the MODEM 11 changes the receiving error display bit of channel status C into "1", and gives a notice of a receiving error of channel block C to the facsimile controller 12.

As described above, transmitting/receiving of controlling channel is processed by using channel blocks B and C. Therefore, even if the receiving/transmitting of controlling channel is operated in full-duplex-simultaneous-mode under V.34 half duplex Standard, the MODEM and facsimile controller do not require complicated processes, but can deliver the transmitted/received data of controlling channel safely. The transmitting/receiving of the main channel works same as that of the controlling channel. Namely, setting a channel-set-mode-bit of the channel command in channel block A at "1" can switch to the transmitting mode, and setting the channel-set-mode-bit of channel block A at "0" can switch to the receiving mode. The transmitting/receiving operation of the main channel can be thus practiced.

Further in V.34 half duplex Standard, a mode switch such as from transmitting/receiving operation of controlling channel to transmitting or receiving operation of the main channel, or vice versa can be executed.

Third, a process of stop the transmitting of data is explained by referring to Fig. 6 – 10. Fig. 6 depicts the relation between the command areas, status areas and banks on the dual port RAM 114. The command areas store instructions about operations sent from the DTE such as channel ending, etc. The status areas store the information about buffer's status such as display of Data Full/Empty, aborts and errors. These areas are provided to each bank in order to strictly control the ending of the processes when each bank completes to transmit data. Each bank stores data in the unit of data-frame which is the unit of error-detection.

Fig. 7 details a bit-map in the command area, and Fig. 8 details a bit-map in the status area. These drawings show the command area and status area corresponding to Bank 0. The same manner can be applied to Bank 1, 2 and 3. Fig. 9 depicts a memory structure showing an interrupt in transmitting. Fig. 10 is a memory structure showing an interrupt in receiving.

Fourth, an operation of the above structure is explained: Regarding the data transmitting process, e.g. Channel A among plural channels is used, the facsimile controller 12 confirms that the display bit of Data Full/Empty of Status 0 is "0", and writes one data-frame of transmitting into Bank 0. When completing the write, the facsimile controller 12 changes the ending-channel-instruction-bit to "0" (not end), and changes the display bit of Data Full/Empty of Status 0 to "1" (WRITE end = READ enable).

When the MODEM 11 recognizes the ending-channel-instruction-bit of Command 0 is "0" and the display bit of Data Full/Empty of Status 0 is "1", the MODEM 11 reads data out of Bank 0 to process signals such as demodulation, and transmits data to line L. When completing to transmit the data out of Bank 0, the MODEM 11 changes the display bit of Data Full/Empty of Status 0 to "0", then simultaneously the interrupt controller 115 produces an interrupt in the facsimile controller 12.

The facsimile controller 12 inspects a transmit-interrupt shown in Fig. 9, thereby notices that the MODEM 11 completed to read the data out of Bank 0. When the display bit of Data Full/Empty of Status 1 corresponding to Bank 1 is "0", the facsimile controller 12, on the other hand, writes the next data-frame into Bank 1 while the MODEM 11 transmits the data of Bank 0. After completing WRITE, the ending-channel-instruction-bit of Command 1 is changed to "1". The MODEM 11 checks Status 1 after completing the transmission of Bank 0, and when the display bit of Data Full/Empty is "1" (in other words, the next data-frame was written-in already), the data of Bank 1 is transmitted as same as Bank 0, and if there is no ending-channel-instruction, the MODEM 11 moves to the next Bank. In the same manner, Bank 2, 3, and 0 in this sequence are transmitted in the unit of data-frame. When ending data-transmitting (channel A), a data-frame is written into e.g. Bank 3, the display bit of Data Full/Empty of Status 3 is changed to "1", and simultaneously the ending-channel-instruction-bit of

Command 3 is changed to "1", thereby the MODEM 11 is given an ending notice. The MODEM 11 checks Status 3 and Command 3 at the same time, whereby recognizes that the display bit of Data Full/ Empty is "1" as well as the ending-channel-instruction, then ends the data transmitting process after transmitting the Bank 3 data.

Fifth, a data receiving process is explained here: The MODEM 11 demodulates the received data, and recognizes the display bit of Data Full/Empty of Status 0 is "0" to write one data-frame into Bank 0. When completing WRITE, the MODEM 11 changes the display bit of Data Full/Empty of Status 0 to "1" (WRITE end = READ enable.) The interrupt controller 115 produces an interrupt on the facsimile controller 12.

The facsimile controller 12 inspects a receiving-interrupt-status, and recognizes that data has been written into Bank 0. When receiving one data-frame, the MODEM 11 checks whether an abort occurs or not, inspects a frame-check-sequence which is added to the frame-end, and judges whether an error exists or not. The judgment is displayed on the receiving-interrupt-status. After confirming no abort exists in the receiving-interrupt-status and also no error in the data-frame, the facsimile controller 12 reads data out of Bank 0. When the display bit of Data Full/Empty of Bank 0 is "0", the MODEM 11 writes the next data-frame into Bank 1 while the data of Bank 0 is read by the facsimile controller 12. After completing WRITE, the data written into Bank 1 is read by the facsimile controller 12, same as the data in

Bank 0. In the same manner, Bank 2, 3 and 0 in this sequence are processed for receiving in the unit of data-frame.

When an error occurs in data-frame or an abort is detected due to line interference in receiving data, how to cancel an error frame is explained by referring to Fig. 11 through Fig. 14: Fig. 11 depicts a status of an error frame being detected when receiving data-frame is checked. Fig. 12(a) depicts a memory where an error-frame is still conventionally stored even the frame has been judged to be an error-frame. Fig. 12(b) depicts a memory where an error-frame is canceled according to this invention.

Fig. 13 depicts a received data where an abort is detected. Fig. 14(a) depicts a memory where the abort frame is still conventionally stored even the frame has been judged having an abort. Fig. 14(b) depicts a memory where the abort frame is canceled according to this invention.

When an error is detected by an error-detecting-signal (frame-check-sequence-error), a frame n (error-frame) is written into Bank 1, and an interrupt is produced in the facsimile controller 12 by the interrupt controller 115. The facsimile controller 12 inspects the receiving-interrupt-status to find that the data has been written into Bank 1 as well as the frame-check-sequence-error has been produced also in Bank 1. The facsimile controller 12 does not read because the data in Bank 1 has an error, and waits the next data-frame.

When receiving the next data-frame n+1, the MODEM 11 does

not write it into Bank 2 but writes it into Bank 1 again as shown in Fig. 12(b). When WRITE is completed, an interrupt is produced on the facsimile controller 12 by the interrupt controller 115. When receiving the interrupt, the facsimile controller 12 inspects the receiving-interrupt-status to find that the next data-frame n+1 has been written into Bank 1, and practices a receiving process. When the abort occurs, same procedures are taken as shown in Fig. 13 and Fig. 14(b).

A mode switch process, the MODEM 11 executes the mode by itself, is explained here by referring to Fig. 15 through Fig. 17. Fig. 15 is a control flow chart depicting an embodiment of this mode switch process according to this invention.

First, the facsimile controller 12 sets a comprehensive mode (S401) which can control a previous and next modes in sequence. Second, the MODEM 11 follows an instruction of executing the comprehensive mode (S402) from the facsimile controller 12, and executes S401 to start processing the previous mode. The facsimile controller 12 then waits for a notice from the MODEM 11 that the previous mode is ended(S403.) When the previous mode is ended, the MODEM 11 gives a notice of ending the previous mode to the facsimile controller 12, and the MODEM 11 sets a timer by itself and monitors a transit time before the next mode is started. When receiving the notice of ending the previous mode, the facsimile controller 12 selects one mode among several modes and instructs the MODEM 11 to execute it in the next mode (S404), then waits for

a notice of ending the next mode from the MODEM 11 (S405). When the timer is out, the MODEM 11 executes the selected mode and monitors the status before giving a notice of ending the next mode to the facsimile controller 12. When receiving the notice of ending the next mode, the facsimile controller 12 ends the sequence of the comprehensive mode.

As explained above, according to this invention, the MODEM 11 automatically executes the mode switch process by simply following the instruction of mode setting from the facsimile controller 12, and there is no need to wait for a mode-switch-instruction or process- start-instruction from the facsimile controller 12. This invention thus prevents a response delay to the next mode even in the procedure where ±5 ms accuracy is required for monitoring the signal-gap-length.

In other words, if the MODEM stores a communication sequence beforehand and the comprehensive mode is set to identify which mode is to be executed, the MODEM can execute the process by itself by controlling a status transition.

Also, according to this invention, the MODEM monitors the timing required until the next mode starts, thereby a delay of switching to the next mode can be avoided even if the case requires ±5 ms accuracy in monitoring the signal-gap-length.

As shown in Fig. 15, this invention proves the following merits: When the process of the previous mode ends at S403, the MODEM 11 controls a status-transition by itself and also the next

mode is set at S404 by the instruction of selecting the next mode, and thereby a timing for mode-switch is guaranteed to secure a safety communication. Further, the MODEM can monitor the timing instead of the facsimile controller 12, whereby reducing the load from the facsimile controller 12.

Various mode-switches by the MODEM are explained. Fig. 16 depicts a meaning that the MODEM 11 has several operation-modes and another operation mode having a sequence which controls the several operation-modes. Fig. 16 is a flow-chart of facsimile sequence using the half-duplex V.34 Standard based on ITU advice. Phase 1 (S431), Phase 2 (S432), Phase 3 (S433), the controlling channel (S434) and the main channel (S435) are the modes in the sequence. The MODEM 11 has the half-duplex mode of V.34 Standard into which these modes are collected.

A MODEM mode is set at V.34 half-duplex mode before the operation is started. Phase 1 of Step S431 starts, where an adjustment is made so that the data based on V.34 Standard can be transmitted/received. When Step S431 is completed, the MODEM 11 transfers to Phase 2 of Step S432 to learn line's characteristics and determines a symbol speed of the MODEM. At Step S433, the MODEM comes into Phase 3 where an equalizer-training (set a coefficient in order to figure out distortion components) to MODEM 11 is provided. After Phase 3, the MODEM comes into Step S434, the controlling channel, where a data speed is determined and terminal information of T.30 Standard is exchanged.

When the controlling channel ends, the MODEM comes into Step S435, the main channel, where image data of the facsimile is transferred. When the main channel ends, the MODEM stays in Step S436 to determine which way to go: by an instruction of facsimile controller 12, to Step S437, the controlling channel which resets a data-speed, or to Step S438, the controlling channel which does not reset a data- speed. For this, the facsimile controller 12 gives an instruction to the MODEM 11 to determine which way to go, Step S437 or S438, before ending the main channel in Step S435.

The MODEM 11 in Step S439, after moving to either Step S437 or Step S438, determines whether the operation ends or not. When the operation does not end, the MODEM returns to Step S435, the main channel, and when the operation ends, the MODEM ends the operation. A non-signal period between Phase 1 and Phase 2 is 75±5 msec, and other non-signal periods between any modes last 70±5 msec. If the facsimile controller 12 controls them, the facsimile controller 12 must bear a heavy load. According to this invention, the MODEM controls them in lieu of the facsimile controller 12 so that the load on the facsimile controller 12 can be reduced.

The above description is for the MODEM 11 to switch the modes by itself (the main channel, transmitting the controlling channel, and receiving the controlling channel.) By referring to Fig. 17 and Fig. 18, an explanation is referred to that the MODEM 11 by itself detects the end of mode shown in S403 and S405 in

Fig. 15. Fig. 17 depicts MODEM mode switching by RCP detection.

This is an example when a facsimile communication or data communication is executed in accordance with V.34 Standard. Fig. 17 shows a timing of mode switching from the main channel upon its completion to the controlling channel mode. Since the facsimile/data communication based on V.34 Standard is operated in ECM mode (error correction mode) whose premise is "error-retransmitting", it is certain that the main channel is to end with an RCP frame which is an end signal of a partial page. If the MODEM can judge the RCP frame in the MODEM, and can switch a mode to the control mode, the MODEM never misses the controlling-channel-signal arriving within 75 ms after the main channel ends. Inside of RCP frame is structured by HDLC-method-framing, and the MODEM 11 must have an ability to execute a deframing operation. After deframing, if data is judged correct, it is easy to judge RCP BYTE.

Another embodiment for the MODEM 11 to switch a mode by itself is explained by referring to Fig. 18. Fig. 18 shows an example of timing in which a facsimile/data communication in accordance with V.34 Standard is operated. In particular, it shows the timing with which the controlling channel mode upon completion is switched to the main channel receiving mode.

Regarding the end of controlling signal, the channel ending signal is specified by a rule of protocol. In this case also, the ending of channel is judged by the MODEM 11 by itself rather than by the facsimile controller 12, thereby switching the mode into

the main receiving mode. To be more specific, the channel ending signal is other than nothing to receive "1" consecutive in not less than 40 bits, which can be detected in the MODEM.

As explained above, the MODEM 11 analyzes the received data by itself, and when the analysis tells that the specified signal has been detected, the MODEM switches a mode based on the result of the detection. The MODEM thus never misses a timing of switch and can guarantee an error-free communication.

Fig. 19 through Fig. 21 depict an instruction process that the MODEM 11 instructs by itself the facsimile controller 12 in a retraining. Fig. 19 is a circuit diagram of MODEM 11, which shows an embodiment of this invention. In Fig. 19, a DTE-interface 617 controls data-transmission such as transmitted/received data as well as other data including instructions of modes, operations, etc. between DTE and MODEM. A transmitted data 613a is sent from the DTE to the other party of communication via the DTE-interface 617. A received data 616a is transmitted from the other party to DTE via the DTE-interface 617. An EQM threshold-value-signal 620b is determined as a reference value for judging a retraining control of MODEM by DTE via the DTE-interface 617. An encoder 613 transduces the transmitted data 613a into two-dimensional-signals 612R and 612I. A QAM modulator 612 provides quadrature amplitude modulation to the two dimensional signals.

The QAM modulator 612 is controlled so that the following signals are output as a modulating signal 612a in response to the

status of a control signal 620c:

In the case of 620c = 0, no signal

620c = 1, quadrature amplitude modulation signal of the two dimensional signals 612R and 612I

620c = 2, training signal

620c = 3, retraining signal

620c = 4, response signal of retraining

A hybrid circuit 611 separates the signals of transmitting system from those of receiving system. This hybrid circuit sends out the transmitted signal 612a to a telephone line 611a, and outputs a received signal 614a from the other party.

A QAM demodulator 614 has two functions, one provides quadrature amplitude modulation to the received signal 614a to output two-dimensional-signal 614R and 614I, the other outputs a judgment of the received signal 614a to a judging signal 620a. The QAM demodulator 614 outputs as follows in response to the status of received signal 614a:

When received signal 614a = no signal, 620a = 0

= data receiving signal, 620a = 1

= training signal, 620a = 2

= retraining signal, 620a = 3

= retraining signal, 620a = 4

A judging part 615 judges the two dimensional signals 614R and 614I. The judged signals 614R and 614I are tapped off from

the judging part 615.

A decoder 616 transduces the judged two dimensional signals 615R and 615I into the received data 616a. An error counter 618 subtracts output signals 615R of judging part 615 from the output signal 614R of QAM demodulator 614, and also subtracts the output signals 615I of the judging part 615 from the output signal 614I of the QAM demodulator 614, then outputs two-dimensional-error-signal 618R and 618I. The EQM calculator 619 calculates a power of the two-dimensional-error-signals 618R and 618I, and then outputs its signal as an EQM signal 619a representing a quality of received data. A controller 620 receives an input consisting of three signals, namely, the EQM signal 619a, the EQM threshold value 620b which is a reference value for retraining, the identifying signal 620a which identifies the received signal, and outputs the control signal 620c to the QAM modulator 612.

Fig. 20 is a block diagram of inside the EQM calculator 619. Multipliers 621 and 622 square the two-dimensional-error-signal 618R and 618I respectively. An adder 623 adds the signals sqaured by the multiplier 621 and 622 and outputs a power signal 623a of the two-dimensional-error. An integrator 624 smoothes the power signal 623a of two-dimensional-error, and outputs the EQM signal 619a representing the quality of receiving data.

Fig. 21 is a flow chart which should be executed in data-receiving-mode by the controller 620 shown in Fig. 19. Step S601 sets the MODEM in waiting status for the training signal to be

detected, and sets the signal 620c to "0" for the QAM modulator 612 to send no signal. Step S602 judges whether the MODEM 11 detects the training signal sent from the MODEM of the other party of the communication or not. When S602 judges "detected", the operation moves to S603, and when "not detected yet", the operation repeats the step S602. When a signal 620a changes to "2", the training signal is judged to be detected. In the step S603, the MODEM is set in training-signal-receiving-status. In step S604, the controller 620 judges whether the training-signal-receiving ends or not. When the training-signal-receiving ends, the operation moves to S605, and when not ends, S604 is repeated. When the signal 620a changes from "2" to "1", the training-signal-receiving is judged to end.

In step S605, the MODEM is set in receiving status, where receiving data is transmitted to the DTE via the QAM demodulator 614, judging part 615, decoder 6161 and DTE-interface 617. Step S606 judges whether the EQM signal 619a representing the quality of receiving data exceeds the EQM threshold value 620b or not. When the EQM signal 619a exceeds the threshold value 620b, the operation moves to step S609, and when the threshold value 620b exceeds the EQM signal 619a, the operation moves to step S607.

Step S607 judges whether data-receiving ends or not. When the data-receiving ends, the operation moves to Step S608, and when not ends, the operation returns to Step S606. The criteria of this judgment whether the data-receiving ends or not is this:

when signal 620a changes from "1" to "0", and when an "end" is instructed by the DTE via the DTE-interface 617.

Step S608 sets the MODEM in data-ending status, and stops the received data to be transmitted to the DTE via the DTE-interface 617, and then moves to an idle mode. Step S609 sets the MODEM in retraining-signal-transmitting status, changes the signal S620c to "3", transmits the retraining signal from the QAM modulator 612, and moves to Step S610. At this moment, the operation temporarily stops the receiving data being transmitted to the DTE via the DTE-interface. Step S610 judges whether the MODEM 11 detects a retraining response signal from the MODEM of the other party of the communication or not. When "detects", the operation moves to Step S601, and when "not detects", the operation repeats Step S610. A criteria of the judgment is this: when the signal 620a changes to "4", it is judged that the retraining signal is detected.

In the above embodiments, retraining is controlled by both the EQM threshold value set by the DTE and the EQM value by the MODEM 11. However, this invention is not limited to these embodiments, but has other structures for controlling the training. For example, a frame-error or bit-error is monitored in the MODEM, and DTE sets a threshold value to the monitoring, thereby the training is controlled. According to the above embodiments, the DTE instructs the EQM threshold value. However, the EQM threshold value may be held by the MODEM before-hand instead.

Next, a process of monitoring the timing by the MODEM is explained. Fig. 22 is a sequence diagram outlining the procedure of V.34 Standard half-duplex mode. First, a timer T1 works as follows: On the receiver side, when the transmitting of ANSam signal starts, at the same time, decrement of the time (e.g. 35 seconds) set in the timer T1 starts. If the timer T1 counts down to "0", the MODEM 11 gives a notice of abnormal by producing an interrupt to the DTE side. However, when a CM signal from a caller is detected before the timer T1 counts down to "0", the decrement in the timer T1 is stopped.

On the caller side, at the same time when receiving the ANSam signal, decrement of time (e.g. 35 seconds) set in the timer T1 provided from the facsimile 12 starts. If the timer T1 counts down to "0", the MODEM produces an interrupt to the DTE side, thereby gives a notice of abnormal. However, a JM signal from the receiver side is detected before the timer T1 counts down to "0", the decrement in the timer T1 is stopped.

It is possible to start the decrements on both sides, i.e. the caller side and receiver side, at the same time when the terminal is linked up to the telephone line.

Second, a timer T2 works as follows: On the receiver side, at the same time when the transmitting of NSF, CSI and DIS signals ends, the decrement of time (e.g. 6 seconds) set in the timer T2 provided from the DTE side starts. If the timer T2 counts down to "0", the MODEM produces an interrupt, thereby gives a notice of

abnormal. However, before the timer T2 counts down to "0", if signals to be appeared TSI and DCS signals could be detected from an address byte to control byte according to HDLC format, then the decrement of timer T2 is stopped and returned to its original time, thereby an interrupt of producing abnormality can be avoided. As explained above, this invention only gives a notice that an abnormality is produced. When an operation is normal, the DTE needs not to be noticed of normality, which does not bother the procedure. Therefore, the method such as a notice is given only when an abnormality occurs, can reduce the load on the facsimile controller 12.

On the caller side, at the same time when transmitting of TSI and DCS signals ends, the decrement of time (e.g. 6 seconds) set in the timer T2 provided from the DTE side starts. If the timer T2 counts down to "0", the MODEM produces an interrupt to the DTE side, thereby gives a notice of abnormal. However, before the timer T2 counts down to "0", if a signal to be appeared CFR signal would be detected from address to control bytes following HDLC format, the decrement of the timer T2 stops and returns to its original time, thereby interrupt of abnormal can be avoided.

The above embodiment handles the timer T2 put in just after Phase B moving from Phase A. Regarding control signals including MPS signal between pages, EOP and MCF signals in Phase B passing through Phase C, the DTE side can monitor the timer 2 with ease by the same method.